AMENDMENTS TO THE CLAIMS

Claim1. (Currently Amended)

A non-volatile passive matrix memory device ~~(10)~~ comprising:

an electrically polarizable dielectric memory material ~~(12)~~ exhibiting hysteresis, particularly a ferroelectric material, wherein said memory material ~~(12)~~ is provided sandwiched in a layer between a first set and second set ~~(14; 15)~~ of respective parallel addressing electrodes, wherein the electrodes of the first set ~~(14)~~ constitute word lines ~~($WL_{1,...m}$)~~ of the memory device and are provided in substantially orthogonal relationship to the electrodes of the second set ~~(15)~~, the latter constituting bit lines ~~($BL_{i,...,}$)~~ of the memory device, wherein a memory cell ~~(13)~~ with a capacitor-like structure is defined in the memory material ~~(12)~~ at the crossings between word lines and bit lines, wherein the memory cells ~~(13)~~ of the memory device constitute the elements of a passive matrix ~~(11)~~, wherein each memory cell ~~(13)~~ can be selectively addressed for a write/read operation via a word line ~~(WL)~~ and bit line ~~(BL)~~, wherein a write operation to a memory cell ~~(13)~~ takes place by establishing a desired polarization state in the cell by means of a voltage being applied to the cell via the respective word line ~~(WL)~~ and bit line ~~(BL)~~ defining the cell, wherein said applied voltage either establishes a determined polarization state in the memory cell ~~(13)~~ or is able to switch between the polarization states thereof, and wherein a read operation takes place by applying a voltage ~~smaller~~ larger than the ~~switching or polarization~~ coercive voltage V_c ~~V_s~~ , to the memory cell

~~(13)~~ and detecting at least one electrical parameter of an output current on the bit lines ~~(BL)~~,

~~characterized in that~~ wherein the word lines ~~(WL)~~ are divided into a number of segments ~~($S_{1,...q}$)~~, each segment ~~comprising~~ including and being defined by a plurality of adjoining bit lines ~~(BL)~~ in the matrix ~~(11)~~, each word line in a segment is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line, where ~~are provided for connecting~~ each bit line ~~(BL)~~ assigned to a segment ~~(S)~~ is connected with an associated sensing means ~~(26)~~, thus enabling simultaneous connection of all memory cells ~~(13)~~ assigned to a word line ~~(WL)~~ on a segment ~~(S)~~ for readout via the corresponding bit lines ~~(BL)~~ of the segment ~~(S)~~, each sensing means ~~(26)~~ being adapted for sensing the charge flow in the bit line ~~(BL)~~ connected therewith in order to determine a logical value stored in the memory cell ~~(13)~~ defined by the bit line.

Claim 2. (Currently Amended)

A non-volatile passive matrix memory device ~~(10)~~ according to claim 1, wherein ~~characterized in that said means (25) for~~ simultaneous connection of each bit line ~~(BL)~~ of a segment ~~(S)~~ with the associated sensing means ~~(26)~~ during addressing is accomplished by ~~are~~ multiplexers.

Claim 3. (Currently Amended)

A non-volatile passive matrix memory device ~~(10)~~ according to claim 2, ~~characterized in that~~ wherein the number of multiplexers ~~(25)~~ corresponds to the largest number of bit lines ~~(BL)~~ defining a segment ~~(S)~~, each bit line of a segment being connected with a specific multiplexer.

Claim 4. (Currently Amended)

A non-volatile passive matrix memory device ~~(10)~~ according to claim 3, ~~characterized in that~~ wherein the output of each multiplexer ~~(25)~~ is connected with a single sensing means ~~(26)~~.

Claim 5. (Currently Amended)

A non-volatile passive matrix memory device according to claim 4, ~~characterized in that~~ wherein the single sensing means ~~(26)~~ is a sense amplifier.

Claim 6. (Currently Amended)

A non-volatile passive matrix memory device according to claim 1, ~~characterized in that said means (25) for~~ wherein simultaneous connection of each bit line ~~(BL)~~ of a segment ~~(S)~~ to an associated sensing means ~~(26)~~ during addressing is accomplished by a gate means.

Claim 7. (Currently Amended)

A non-volatile passive matrix memory device according to claim 6, ~~characterized in that~~ wherein all bit lines ~~($BL_{1,...n}$)~~ of a segment ~~(S)~~ are connected with a specific gate means, each gate means having a number of outputs corresponding to the number of bit lines ~~(BL)~~ in the respective segment ~~(S)~~, that each output of each gate means ~~(25)~~ is connected with a specific bus line ~~(27)~~ of an output data bus ~~(28)~~, the number of bus lines ~~(27)~~ thus corresponding to largest number of bit lines ~~(BL)~~ in a segment ~~(S)~~, and that each bus line ~~(27)~~ is connected with a single sensing means ~~(26)~~.

Claim 8. (Currently Amended)

A non-volatile passive matrix memory device according to claim 6, ~~characterized in that~~ wherein the gate means ~~(25)~~ comprise pass gates.

Claim 9. (Currently Amended)

A non-volatile passive matrix memory device according to claim 6, ~~characterized in that~~ wherein the sensing means ~~(26)~~ is a sense amplifier.

Claim 10. (Withdrawn)

A method for readout of a non-volatile passive matrix memory device (10) comprising an electrically polarizable dielectric memory material (12) exhibiting hysteresis, particularly a ferroelectric material, wherein said

memory material (12) is provided sandwiched in a layer between a first set and second set (14;15) of respective parallel addressing electrodes, wherein the electrodes of the first set (14) constitute word lines (WL) of the memory device (10) and are provided in substantially orthogonal relationship to the electrodes of the second set (15), the latter constituting bit lines ($BL_{1,...n}$) of the memory device (l0), wherein a memory cell (13) with a capacitor-like structure is defined in the memory material (12) at crossings between word lines (WL) and bit lines (BL), wherein the memory cells (13) of the memory device (10) constitute the elements of a passive matrix (11), wherein each memory cell (13) can be selectively addressed for a write/read operation via a word line (WL) and bit line (BL), wherein write operation to a memory cell (13) takes place by establishing a desired polarization state in the cell by means of a voltage being applied to the cell via the respective word line (WL) and bit line (BL) defining the cell, said applied voltage either establishing a determined polarization state in the cell or being able to switch the cell between the polarization states thereof, wherein a read operation takes place by applying a voltage smaller than the switching or polarization voltage V_s to the memory cell (13) and detecting at least one electrical parameter of an output current on its bit lines (BL), and wherein the method comprises steps for controlling electric potentials on all word lines (WL) and bit lines (BL) in a time-coordinated fashion according to a protocol comprising electric timing sequences for all word lines and bit lines, arranging said protocol to comprise

a read cycle, and providing during the read cycle for the sensing means to sense charges flowing in the bit lines, and wherein the method is characterized by dividing the word lines (WL) into a number of segments ($S_1,...S_q$), each segment comprising and being defined by a number of adjacent bit lines (BL) in the matrix (11), connecting each bit line (BL) within a word line segment (S) with an associated sensing means (26), activating according to the protocol one word line (WL) of a segment (S) at a time by setting the potential of said one word line (WL) of the segment (S) to the switching voltage V_s, during at least a portion of the read cycle, while keeping all bit lines of the segment (S) at zero potential, and determining the logical value stored in the individual memory cells (13) sensed by the sensing means (26) during the read cycle.

Claim 11. (Withdrawn)

Method for readout according to claim 10, characterized by keeping all word lines (WL) and bit lines (BL) when no memory cell (13) is read or written, at a quiescent voltage of approximately □ of the switching voltage V_s, activating according to the protocol one word line (WL) at a time by setting the potential of said one word line (WL) of the segment (S) to the switching voltage V_s, during at least a portion of the read cycle, while keeping all bit lines (BL) of the segment (S) at zero potential, and

determining the logical value stored in the individual memory cells (13) sensed by the sensing means (26) during the read cycle.

Claim 12. (Currently Amendment)

~~The use of a non-volatile passive matrix memory device (10) according to claim I and a method for readout according to claim 10 in a~~

A volumetric data storage apparatus comprising: ~~with~~

a plurality of stacked layers ~~(P_1, P_2,...)~~, each layer ~~(P) comprising~~ including one ~~of the~~ non-volatile passive matrix memory device, the non-volatile passive matrix memory device including an electrically polarizable dielectric memory material exhibiting hysteresis, particularly a ferroelectric material,

wherein said memory material is provided sandwiched in a layer between a first set and second set of respective parallel addressing electrodes,

wherein the electrodes of the first set constitute word lines of the memory device and are provided in substantially orthogonal relationship to the electrodes of the second set, the latter constituting bit lines of the memory device,

wherein a memory cell with a capacitor-like structure is defined in the memory material at the crossings between word lines and bit lines,

wherein the memory cells of the memory device constitute the elements of a passive matrix, wherein each memory cell can be selectively addressed for a write/read operation via a word line and bit line, wherein a write operation

to a memory cell takes place by establishing a desired polarization state in the cell by means of a voltage being applied to the cell via the respective word line and bit line defining the cell,

wherein said applied voltage either establishes a determined polarization state in the memory cell or is able to switch between the polarization states thereof, and wherein a read operation takes place by applying a voltage smaller than the switching or polarization voltage V_s, to the memory cell and detecting at least one electrical parameter of an output current on the bit lines,

wherein the word lines are divided into a number of segments, each segment including and being defined by a plurality of adjoining bit lines in the matrix, each word line in a segment is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line, where each bit line assigned to a segment is connected with an associated sensing means, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment, each sensing means being adapted for sensing the charge flow in the bit line connected therewith in order to determine a logical value stored in the memory cell defined by the bit line. ~~devices (10)~~.

Claim 13. (New)

A memory device, comprising:

a first set of electrodes which constitute word lines of the memory device;

a second set of electrodes which constitute bit lines of the memory device, the second set of electrodes being positioned substantially orthogonal to the first set of electrodes, the bit lines being divided into a number of segments;

an electrically polarizable dielectric memory material provided in a layer between the first and second set of electrodes, the electrically polarizable dielectric memory material and the first and second set of electrodes forming a passive matrix memory in which each memory cell can be selectively addressed for a write/read operation; and

a number of sensing devices connected to each of a corresponding bit lines within each segment of word lines, where each word line in each segment is differentiated based on the position of the word line within the segment, each word line of each segment being adjoined to a separate bit line, thus enabling simultaneous connection of all memory cells assigned to a segment.

AMENDMENTS TO THE DRAWINGS

Attached hereto (are) eight (8) sheets of corrected formal drawings that comply with the provisions of 37 C.F.R. § 1.84. The corrected formal drawings incorporate the following drawing changes:

Figs. 1-4 alleging that they should be labeled as "PRIOR ART". In response, applicants have labeled Figs. 1-4 as "CONVENTIONAL ART" which is how they are described in the specification.

The Office Action also states that the line on the right side of each of the figures interferes with some of the figure drawings and text and should be removed. In response, applicants have removed the line on the right side of the figures.

It is respectfully requested that the corrected formal drawings be approved and made a part of the record of the above-identified application.